ABSTRACT

A computer system has a processor that has a prediction array that avoids conflicts when the prediction array is accessed twice in once clock cycle to retrieve predictions for two separate conditional branch instructions. The prediction array is included as part of a branch prediction logic circuit that includes a bank control logic coupled to the prediction array. The bank control logic assures the conflict noted above is avoided. The prediction array preferably comprises multiple (*e.g.*, 4) single-ported bank memory elements, each bank comprising multiple predictions. The bank control logic uses information associated with a previously fetched and branch predicted conditional branch instruction to generate a bank number for a current branch instruction. The generated bank number corresponds to one of the banks in the prediction array. The processor preferably fetches two (or more) groups (also called "slots") of instructions each cycle. Each slot may include one or more branch instructions that need to be branch predicted. Thus, the branch prediction logic circuit first generates a bank number for one of the slots and then generates a bank number for the other slot and uses the bank numbers to retrieve predictions from the multi-bank, single ported prediction array. The bank control logic computes the bank numbers in a manner that assures that no two consecutively generated bank numbers are identical.